FIG. 1

$F_0/R \cdot N$

OUTPUT SIGNAL

10

F_0

12
$\div R$

$F_0/R1$

16
ϕ

15
FILTER

18
VCO

20
VARIABLE DIVIDER N OR N+1

N

14

21
FRACTIONAL CONTROL CIRCUIT

21

Carry Out 27

25

Input
→ Accumulator

n-bits

26

Delay

n-bits
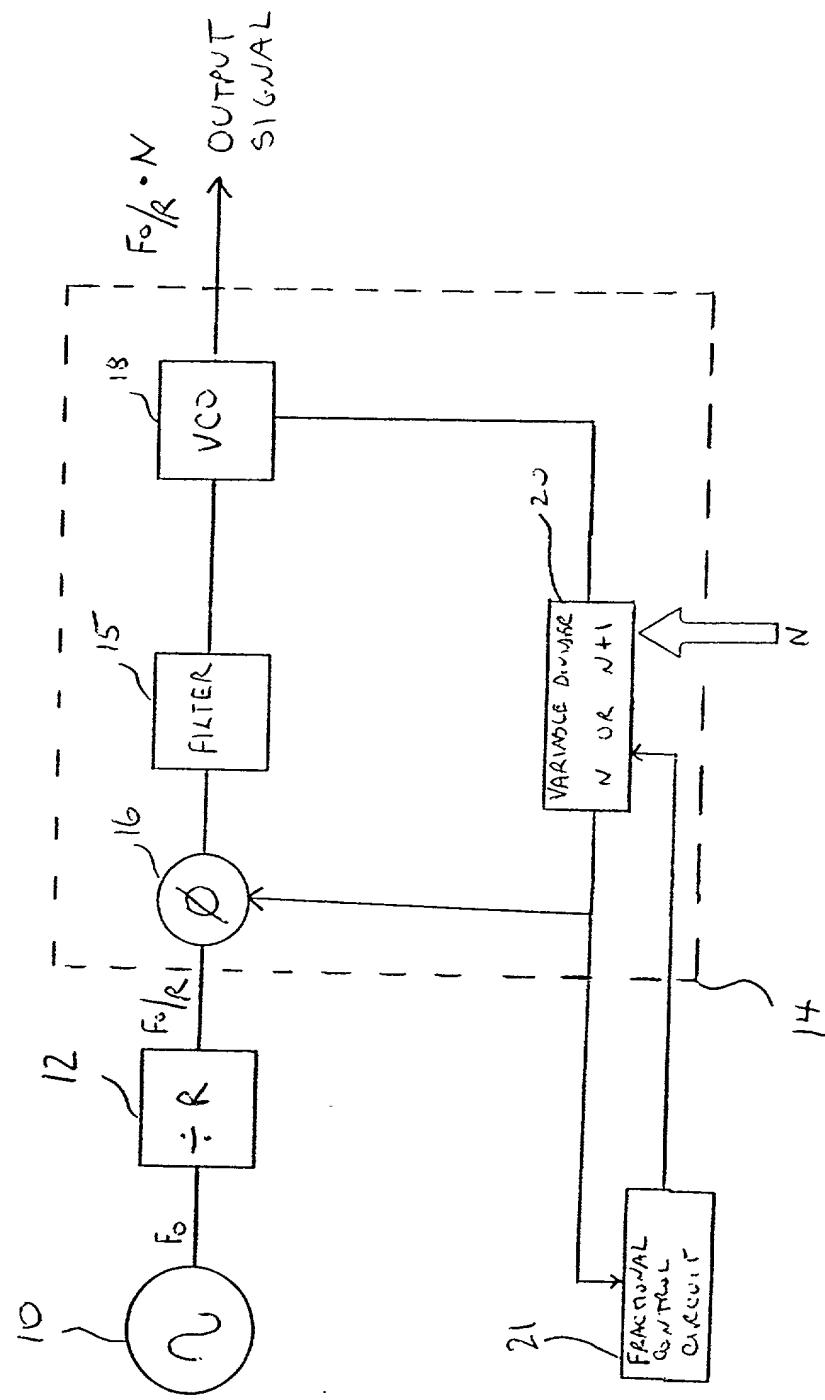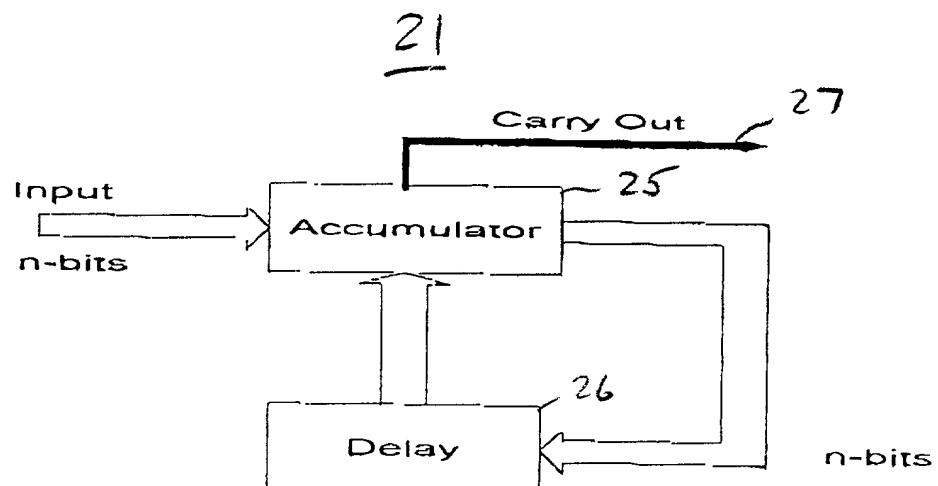
PRIOR ART

FIG.2

30

FIG. 3

4th ORDER DELTA SIGMA INTERPOLATOR
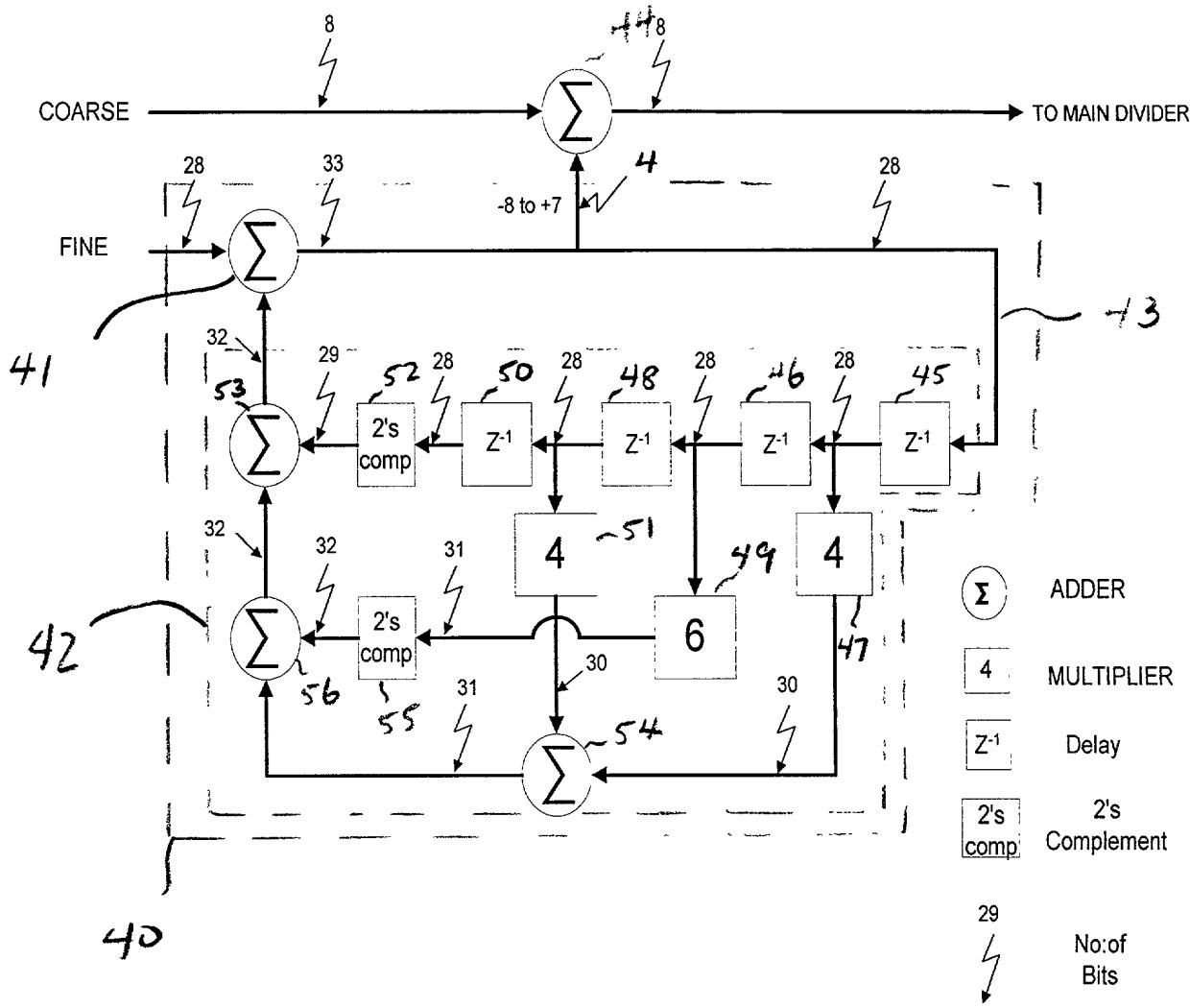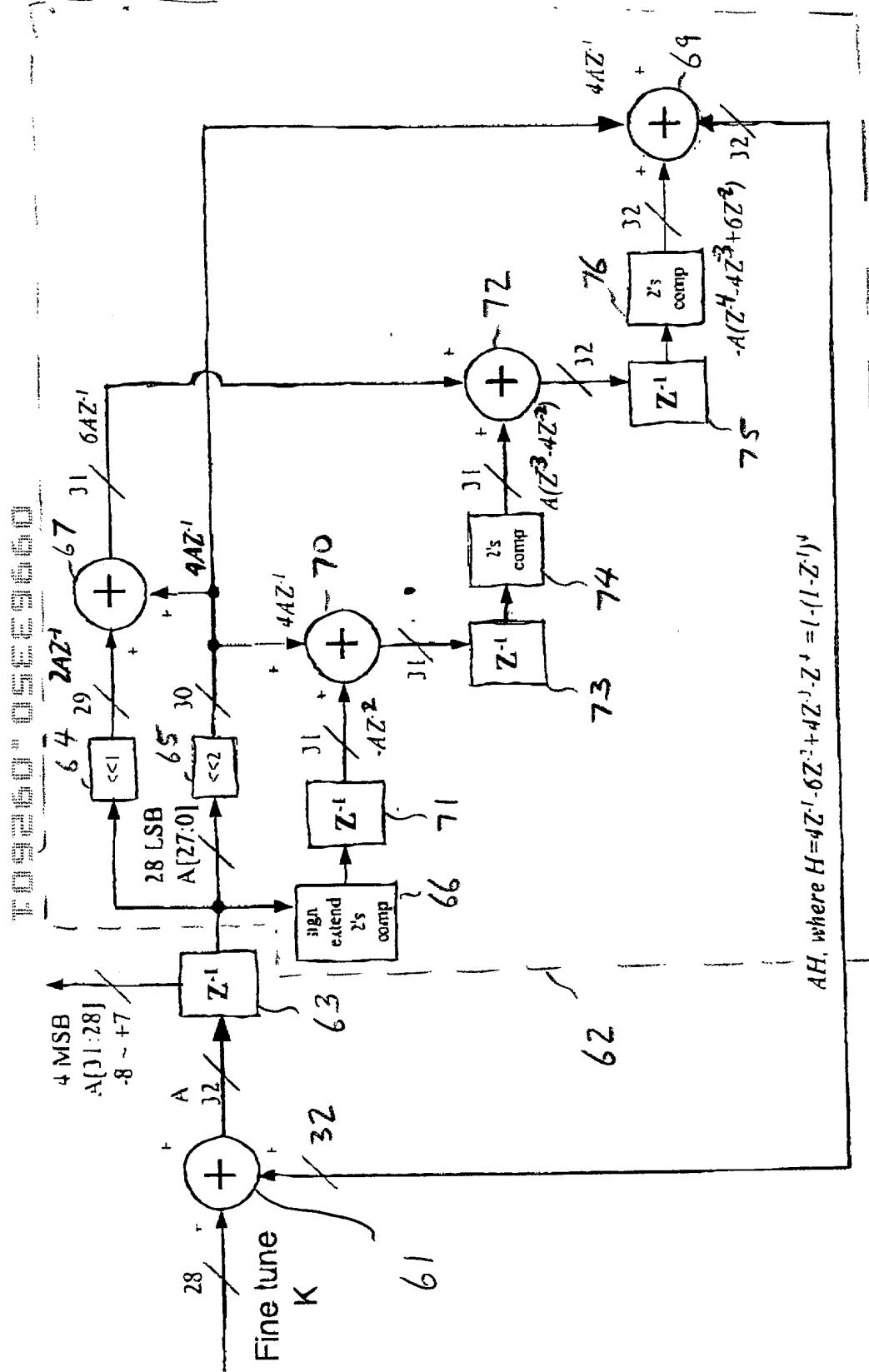

FIG. 4

4 MSB
A[31:28]
-8 ~ +7

A
/32

28 ──┼──
+ ──○── Z⁻¹ ──┼──
Fine tune │
K │ 63
/32

61

67
/31 6AZ⁻¹
2AZ⁻¹
64 29 /31
<<1 ──○──+ ──
+

28 LSB
A[27:0]

65 30
<<2

4AZ⁻¹

66
sign
extend 2's
comp

71
Z⁻¹ -AZ²
/31

70
4AZ⁻¹
+ ──○──+ ──
/31

73
Z⁻¹

74
2's
comp A(Z⁻³-4Z⁻²)
/31

72
+ ──○──+ ──/32
+

75
Z⁻¹ -A(Z⁻⁴-4Z⁻³+6Z⁻²)
/32

76
2's
comp
/32

69
4AZ⁻¹
+ ──○── +
+ /32

62

AH, where H=4Z⁻¹-6Z⁻²+4Z⁻³-Z⁴=1-(1-Z⁻¹)⁴

69

FIG.5